CURRENT MIRROR COMPENSATION CIRCUIT AND METHOD

TECHNICAL FIELD

The circuitry described herein relates generally to automatic test equipment, and more particularly low jitter timing generation circuits for automatic test equipment applications.

BACKGROUND

Timing edge placement is often a critical parameter for high performance semiconductor testers. Having the ability to place the rising and/or falling edge of a test signal within a few picoseconds of a desired point in time may mean the difference in passing or failing large numbers of semiconductor devices under test.

Conventional timing generators that produce high accuracy timing signals are often employed in CMOS integrated circuits. CMOS technology provides relatively good performance at very low cost. However, CMOS ICs are often susceptible to temperature and other conditions that affect the performance of the circuit. To counter this, many CMOS timing generators employ sophisticated compensation techniques to minimize changes in delay.

With reference to Figure 1, a conventional CMOS timing generator 10 that provides for temperature compensation typically includes a plurality of delay elements D1 - DN coupled together to form a delay line. Each of the delay element outputs serve as timing selection inputs to a timing signal selector (not shown). The same outputs are also used for a delay compensation scheme. A compensation multiplexer 12 is employed, that receives the delay outputs, and provides an output to a phase detector 14, where it is compared to a reference signal Vref to determine any phase difference. A compensation voltage is then generated in response to the magnitude of any phase difference, and fed to a charge pump or voltage-to-current converter 16. The current generated by the converter is provided as a reference bias current to a bias current fanout circuit 18 that duplicates and distributes bias current to the delay elements to control the delay.

To fanout, or distribute the bias current to the various delay elements, a current mirror circuit scheme is typically employed. As shown in Figure 2, a conventional current mirror includes a reference current source 19 coupled to a current source transistor Q_S to generate the same current through a first mirror transistor Q_{FM}. The

mirror transistor's gate is tied to its drain, with its source terminal coupled to the supply voltage VDD. A plurality of mirroring transistors QFM2 - QFMN are disposed in parallel, each with its gate tied to the first mirror transistor gate, and source terminals tied to VDD.

While this configuration works well for its intended applications, the current through each mirror transistor may be susceptible to noise components acting on the VDD bus. Even a relatively small change of 100 millivolts can cause a corresponding change in the bias current through each mirror, correspondingly affecting the level of current provided therefrom. As voltage levels on integrated circuits continue to decrease, this problem becomes more pronounced.

What is needed and currently unavailable is a compensation circuit for use with current mirror circuits to minimize changes in current attributable to supply voltage noise. The current mirror compensation circuit described herein satisfies this need.

SUMMARY

The current mirror compensation circuit described herein provides a low-jitter solution for the generation of bias currents by one or more current mirrors. By minimizing the errors attributable to noise in the supply voltage, reduced supply voltage levels may be employed in integrated circuits with little error caused by the current mirror circuitry.

To realize the foregoing advantages, the circuit in one form comprises a current compensation circuit for use with a current mirror. The current mirror circuit has a current path defined by a first current mirror stage driving a second current mirror stage, the second current mirror stage is coupled to a supply voltage source. The current compensation circuit comprises an impedance divider coupled to the supply voltage and an output node. The impedance divider operates to generate a compensation signal at the node representative of voltage changes in the supply voltage source. The compensation circuit further includes a gain stage having an input coupled to the output node and a current output connected to the current path. The gain stage operates to generate a compensation current for application to the current path in response to the compensation signal.

In another form, the circuit comprises a timing generator for use in a semiconductor tester. The timing generator includes a delay line having a plurality of delay cells with respective phase-shifted outputs and bias current inputs. A selector with a plurality of inputs receives the phase shifted outputs, and includes an output. Phase detection circuitry detects the phase shift between the selector output and a reference signal, and generates bias current. The timing generator further includes means for distributing the bias current to the plurality of delay cells.

Other features and advantages of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The circuit described herein will be better understood by reference to the following more detailed description and accompanying drawings in which

FIG. 1 is a high-level block diagram of a conventional timing generator;

FIG. 2 is a partial schematic view of the conventional bias current fanout circuitry employed in the timing generator of Figure 1;

FIG. 3 is a high-level block diagram of a timing generator according to one form of the circuit described herein; and

FIG. 4 is a high-level block diagram of a bias current source for use in the timing generator of Figure 3.

DETAILED DESCRIPTION

The current mirror compensation circuit described herein, generally designated 50, provides a unique solution for addressing the undesirable effects of a changing supply voltage in high performance CMOS timing generators. This is accomplished by feeding compensation current to bias current generated by fanout circuitry 30. The compensation current offsets any changes to the bias current resulting from any changes in VDD caused by noise or jitter. By minimizing the effects of a changing VDD, changes to the delay characteristics of the cell are also correspondingly minimized.

Referring now to Figure 3, a timing generator that employs the current mirror compensation circuit, generally designated 20, is shown. The timing generator is of the type that provides bias current compensation to control delay. The generator includes a delay line 22 comprising a set of N delay elements D1 - DN, each providing a proportional to 1/N phase offset with respect to an input clock CLK. A preferred delay element construction that provides low jitter delay is described in co-pending patent application serial number 10/376,664, titled "Low Jitter Delay Cell", filed February 28, 2003, assigned to the assignee of the present invention, and expressly incorporated by reference herein.

Further referring to Figure 3, the delay element outputs are fed to a selector, or multiplexer M1. The multiplexer output feeds a phase detector 24 that determines the phase difference between the selected delay signal (presented by the multiplexer) and a reference signal Vref. A charge pump and voltage-to-current converter 26 receives a difference signal from the phase detector to generate a reference bias current IREF. The reference bias current is then duplicated and distributed by fanout circuitry 30 to provide the bias current for the delay elements. The change in bias current serves to control the delay through each element to a desired level.

Referring now to Figure 4, the fanout circuitry 30 generally includes a reference current source input transistor QIN1 that receives an off-chip current IOC to generate a bias voltage for a first current mirror CM1. The first current mirror is in the form of a current DAC having transistors QM1A - QM1N. As is well understood in the art, the current DAC comprises a bank of transistors that are selectively activated to achieve desired characteristics.

With continued reference to Figure 4, the first current mirror CM1 (transistor DAC QM1A - QM1N) is disposed in series with a second current mirror CM2 comprising transistor QM2, forming a node with QM2 at 40. While not explicitly

shown in Figure 4, the voltage-to-current converter output (Figure 3) is connected to node 40. The second current mirror transistor Q_{M2}, in turn, has its gate tied to the gates of an array of mirror transistors Q_{M3} - Q_{MN}. Because of the respective gate-to-source connections for each transistor, the current through Q_{M2} is duplicated en masse through transistors Q_{M3} - Q_{MN}. The duplicated currents are then fed as bias currents to the delay cells, or groups of delay cells.

For optimum control over the bias current, and to minimize the effects from undesirable changes on the supply voltage VDD, the fanout circuitry 30 includes an input, at node 40, for receiving compensation current from the current mirror compensation circuit 50.

Referring again to Figure 4, the current mirror compensation circuit 50 comprises an impedance divider 52 and a programmable common source gain stage 54. The impedance divider is preferably in the form of a voltage divider with a pair of series-connected resistors R1 and R2. In the overall preferred implementation wherein the entire fanout and compensation circuitry is disposed on a single CMOS integrated circuit, the resistors take the form of diode-connected MOSFET transistors having channel configurations corresponding to desired resistances of approximately one to two kohms. The resistors form a path from the supply voltage source V_{DD}, at one end, to the return voltage rail, or ground, at the other end. An output node disposed at the junction between R1 and R2 provides a reduced-voltage output for application to the programmable current source 54.

The programmable common source gain stage 54 comprises a parallel array of P-channel MOS transistors Q_{P1} - Q_{PN} that are programmable to enable a varying range of current gain in response to a range of detected voltages at the divider output node. In other words, the range of available current in response to a sensed voltage from the divider may be increased or decreased depending on how many transistors from the array are activated.

To provide a programmable bias current for the common source gain stage 54 over the compensation current, an array of n-channel transistors Q_{N1} - Q_{NN} are coupled to the p-channel array. Each gate terminal of the n-channel array is tied to the first current mirror CM1. Like the p-channel array, the n-channel transistors may be programmably activated as necessary to generate the desired bias current. The output of the programmable gain stage 54 feeds the fanout circuitry input at node 40.

In operation, the accuracy of the timing generator 20 (Figure 3) depends upon the accuracy of the individual delays associated with each delay cell DN. The

individual delays are each regulated by the bias current running through each cell DN. Bias current is drawn through each cell and is programmed by the user to achieve the desired delay for the cell. Generally, a higher bias current results in a shorter delay, while a lower bias current increases the delay. The bias voltage for the cell is provided by the V_{DD} bus, generally on the order of 1.2 volts. However, noise often affects the value of V_{DD}, sometimes increasing or decreasing the level by +/- 0.10 volts.

Where a noisy VDD affects the bias current produced by the fanout circuitry 30, the compensation current circuit 50 offsets the effect by sinking or sourcing appropriate levels of current into the input node 40 (Figure 4). In the instance where too much current is being drawn through the second current mirror CM2 because of a noisy VDD, additional current is supplied into the node 40 from the compensation circuit 50, causing transistor QM2 to supply correspondingly less current, while the first current mirror CM1 (transistor QM1) still draws its required current. In the instance where too little current is drawn through transistor QM2, the compensation circuit sinks current, forcing QM2 to provide additional current, which is duplicated through mirror transistors QM3 - QMN. The programmability aspect of the current mirror compensation circuit allows for fine tuning the compensation current, as necessary.

Those skilled in the art will appreciate the benefits and advantages afforded by the circuit described herein. Of significant importance is the current compensation feature that offsets bias current inaccuracies caused by undesirable noise acting on the supply voltage. Further, the programmable nature of the circuit provides flexibility and accuracy in allowing for fine-tuning of the compensation current. Moreover, due to the circuit's convenient construction, it is readily adaptable for use as a standard cell block.

It will also be appreciated that the current mirror compensation circuit described herein is not limited solely to the field of automatic test equipment (ATE). While ATE presents a challenging environment where such a circuit provides a substantial beneficial impact, any application where current mirroring techniques are employed may benefit from the use of this circuit. For example, circuits that employ analog-to-digital conversion techniques or where current generates a reference voltage may use the compensation circuit. These applications are likely to use current mirroring techniques with reduced supply voltages.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.